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10/809,800	03/26/2004	Haruhiko Murata	65933-080	7161

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MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
NADKARNI, SARVESH J	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,800	MURATA ET AL.	
	Examiner	Art Unit	
	Sarvesh J. Nadkarni	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/06/2006 and 03/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed March 26, 2004, Application Number: 10/809,800 (hereinafter referred to as "application"). The application was published on December 2, 2004, Publication Number: US 2004/0239587. Page and line number references made in this action relate to the originally filed application, not the publication. Receipt is acknowledged of the information disclosure statement, form PTO-892, filed on March 26, 2004 and September 6, 2006.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 10 is objected to because of the following informalities: the element "**adjoining-pixel difference absolute values**" in line 6 of the application is not introduced using proper antecedent basis format; the article "a" or "an" is used to introduce an element, whereas "the" or "said" is used to refer to a previously introduced element or step. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 3, 14, 17, 18, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Arita et al, United States Patent Application Publication, Publication Number: 2003/0020681 A1, Publication Date: January 30, 2003 (hereinafter referred to as "Arita").

5. With regard to claim 1, Arita clearly discloses **a display processor** (see page 6 paragraph [101] "CDE processing circuit 14") **comprising: a first obtaining unit** (see FIG. 6 Average calculation 134, and further described on page 9, paragraph [0128]) **which obtains an average pixel value, or an average of pixel values** (see FIG. 6 Average calculation 134, and further described on page 9, paragraph [0128]) **in a predetermined area on a line** (see FIG. 2A; Xn-1, Xn and Xn+1 in a predetermined area on a line); **an operation unit which calculates a pixel difference value** (see FIG. 6 Difference calculation 135, and as further described on page 9, paragraph [0128]), **or a difference between the average pixel value** (see FIG. 6, Average calculation outputs the average pixel value to difference calculation) **and a pixel value of a target pixel to be corrected** (see page 9, paragraph [0128] describing the predetermined pixel "Xn to be corrected"); **a processing unit which corrects the target pixel value** (see FIG. 6 comparison circuit 142 and as further described in paragraph [0128]), **or the pixel value of the**

target pixel, according to the pixel difference value(see FIG. 6 comparison circuit 142 and as further described in paragraph [0128]); **and a display unit which displays the pixel value corrected** (see FIG. 1, liquid crystal display panel unit 11).

6. With regard to claim 2, Arita clearly discloses **the display processor according to claim 1, wherein the processing unit comprises a second obtaining unit** (see page 10 paragraph [0143] second comparison section 42) **which obtains a variation in pixel value near the target pixel** (see page 10, paragraph [0149] describing the delta or variation near a target pixel; furthermore see FIG. 9); **and a correction unit** (see page 10, paragraph [0145] "selection section 44") **which corrects the target pixel value according to the variation** (the selection section 44 selects the correct output from the LSB determination section 43, see paragraph [0145]).

7. With regard to claim 3, Arita clearly discloses **the display processor according to claim 2, wherein the processing unit decreases the amount of correction of the target pixel value with an increasing variation** (see page 12, paragraph [0174], "sets the LSB to 0 when the difference value is equal to or greater than the predetermined reference value"), **and increases the amount of correction of the target pixel value with a decreasing variation** (see page 12, paragraph [0174] "sets the LSB to 1 when the difference value is smaller than the predetermined reference value").

8. With regard to claim 14, Arita clearly discloses **the display processor according to claim 1, wherein the processing unit corrects the target pixel value according to the position of the target pixel on the display unit** (see page 10, paragraph [0146] through [0150] describing the correction of pixel Xn, the target pixel, according to its position).

9. With regard to claim 17 and 19, they are similarly analyzed as claim 1 and rejected under the same rationale.

10. With regard to dependant claims 18 and 20, they are similarly analyzed as claim 2 and rejected under the same rationale.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita as applied to claims 2 and 3 above, and further in view of Kanai et al., United States Patent, Patent Number: U.S. 6,590,617 B1, Date of Patent: July 8, 2003, filed February 22, 2000 (hereinafter referred to as "Kanai '617").

13. With regard to claim 4, Arita discloses **the display processor according to claim 2.** However, Arita fails to teach **the second obtaining unit obtains the variation based on adjoining-pixel difference absolute values, or absolute values of differences between the pixel values of pixels adjoining within a certain area near the target pixel.**

14. Kanai '617 clearly teaches **the second obtaining unit** (see column 2, line 17, "first computation means" **obtains the variation based on adjoining-pixel difference absolute values** (see column 2, lines 17-19, the first computation means computes absolute values of differences between neighboring pixels and pixel of interest), **or absolute values of differences**

between the pixel values of pixels adjoining within a certain area (see column 2, lines 17-19) **near the target pixel** (see column 2, line 18, "pixel of interest").

15. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate first computation means of Kanai '617 into the display correction apparatus of Arita because both device are within the same field of endeavor and Kanai '617 improves image sharpness near the edges (see Kanai '617 column 1, lines 12-13), a progressively common goal within the art and shared by both references.

16. With regard to claim 5, it is similarly analyzed as claim 4 above and rejected under the same rationale.

17. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita in view of Kanai '617 as applied to claims 4 and 5 above, and further in view of Willis et al., United States Patent Number US 6,647,152 B2, Date of Patent: November 11, 2003, filed January 25, 2002 (hereinafter referred to as "Willis '152").

18. With regard to claim 6, Arita in view of Kanai '617 teaches **the display processor according to claim 4, the second obtaining unit, and the adjoining-pixel difference absolute values.** However, Arita in view of Kanai '617 fails to teach **the variation based on an integrated value.**

19. Willis '152 clearly teaches **obtaining the variation based on an integrated value** (see column 4, lines 43-63, the contouring detection process 300 determines an integrated value by including all values in a predetermined span of pixels into its variation determination).

20. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the variation determination system

as taught by Willis '152 into the processor of Arita in view of Kanai '617 because they are in the same field of endeavor, an furthermore, Willis '152 improves the "stair step" effect and creates a smoother image, a common goal with the art (see column 1, lines 23-25).

21. With regard to claim 7, it is similarly analyzed as claim 6 above and rejected under the same rationale.

22. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita in view of Kanai '617 as applied to claims 4 and 5 above, and further in view of Kasahara et al., United States Patent Number: US 6,812,932 B2, Date of Patent: November 2, 2004, filing date: July 30, 2001 (hereinafter referred to as Kasahara '932).

23. With regard to claim 8, Arita in view of Kanai '617 discloses **the display processor according to claim 4, an adjoining-pixel difference absolute value, and the second obtaining unit.** However, Arita in view of Kanai '617 fail to teach that if **the adjoining-pixel difference absolute value exceeds a threshold, the second obtaining unit determines an integrated value by subjecting the threshold to the integration instead of the adjoining-pixel difference absolute value.**

24. Kasahara '932 clearly teaches that **if an adjoining-pixel difference absolute value** (see column 28, lines 60-63 "difference in luminance (absolute value) between a certain pixel and adjacent thereto") **exceeds a threshold** (see column 29 lines 6-10 "fourth predetermined value"), **the second obtaining unit** (see column 28, lines 59-60, "edge detector 64c") **determines an integrated value** (see column see column 29 line 12 "4x4" pixel area) **by subjecting the threshold to the integration instead of the adjoining-pixel difference absolute value** (see the example at column 29, lines 10-13).

25. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate edge detector of Kasahara '932 into the processor of Arita in view of Kanai '617 because both are in the same field of endeavor and furthermore, Kasahara '932 aims to reduce pseudo-contour noise (see column 3, lines 21-27), a common goal in the art.

26. With regard to claim 9, it is similarly analyzed as claim 8 above and rejected under the same rationale.

27. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita as applied to claim 1 and 3 above, and further in view of Kasahara '932.

28. With regard to claim 10, Arita discloses **the display processor according to claim 2 and also the second obtaining unit.** However, Arita fails to disclose that **the second obtaining unit compares each of the adjoining-pixel difference absolute values between adjoining pixels within a certain area near the target pixel with a threshold, and obtains the variation based on the counted number of adjoining-pixel difference absolute values exceeding the threshold.**

29. Kasahara '932 discloses **the second obtaining unit** (see column 28, lines 59-60, "edge detector 64c") **compares each of the adjoining-pixel difference absolute values between adjoining pixels** (see column 28, lines 60-63 "difference in luminance (absolute value) between a certain pixel and adjacent thereto") **within a certain area** (see column 28, lines 60-63 "a pixel adjacent thereto in each of a vertical, horizontal and diagonal directions") **near the target pixel** (see column 28, line 61"certain pixel") **with a threshold** (see column 29 lines 6-10 "fourth predetermined value" which is compared to the differences determined for each pixel), **and**

obtains the variation based on the counted number of adjoining-pixel difference absolute values exceeding the threshold (see column 29, lines 9-10, edge determined based on those values exceeding the fourth predetermined value).

30. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the edge detector as taught by Kasahara '932 into the display correction apparatus of Arita because both are in the same field of endeavor, and furthermore, Kasahara '932 aims to reduce pseudo-contour noise (see column 3, lines 21-27), a common goal in the art.

31. With regard to claim 11, it is similarly analyized as claim 10 above and rejected under the same rationale.

32. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita in view of Kanai '617, and further in view of Kasahara '932.

33. With regard to claims 12 and 13, they are similarly analyzed as claim 10 above and rejected under the same rationale.

34. Claims 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arita as applied to claim 1 above, and further in view of Willis '152.

35. With regard to claim 15, Arita teaches **the display processor according to claim 1.** However, Arita fails to teach that **the first obtaining unit obtains the averages or integrated values of the pixel values in predetermined areas on a plurality of lines including the predetermined area on the line, the operation unit calculates a line difference value, or a difference between the average pixel values or integrated values of the lines, and the processing unit corrects the target pixel value according to the line difference value.**

36. Willis '152 clearly teaches **the first obtaining unit** (see column 5, lines 3-5 "processor 70") **obtains the averages or integrated values** (see column 5 lines 3-5, "processor 70 calculates the average pixel component value of the predetermined pixel span") **of the pixel values in predetermined areas** (see column 5, lines 3-5, "pixel span") **on a plurality of lines** (see FIG. 8 and FIG. 9, further described in column 5, lines 36-40, furthermore, see column 5, lines 13-15) **including the predetermined area on the line** (see column 5, lines 3-5), **the operation unit calculates a line difference value** (see column 4, lines 53-56), **or a difference between the average pixel values or integrated values of the lines** (see column 4, lines 53-56), **and the processing unit** (see column 4, lines 61-68, contour reduction process 400) **corrects the target pixel value according to the line difference value** (see column 4, lines 61-68).

37. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the system as taught by Willis '152 into the display processor of Arita because both are in the same field of endeavor and furthermore, Willis '152 improves the "stair step" effect and creates a smoother image, a common goal with the art (see column 1, lines 23-25).

38. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arita as applied to claim 1 above.

39. With regard to claim 16, Arita fails to teach that **when the display unit is split into a plurality of areas for driving, the processing unit corrects the pixel value of a pixel at a position symmetrical to the target pixel in the split area.**

40. However it would it would have been obvious to one having ordinary skill in the art at the time the invention was made to symmetrically correct a symmetrically split display unit

because simultaneous correction was already known at the time of invention and this would be an obvious variation of such correction.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarvesh J. Nadkarni whose telephone number is 571-270-1541. The examiner can normally be reached on 8:00-5:00 M-Th EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-273-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJN

XIAO WU
SUPERVISORY PATENT EXAMINER